REMARKS

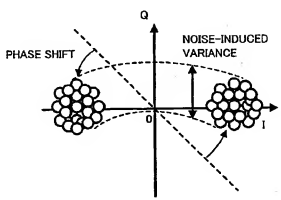
The Office Action indicated that Claims 21-23 were allowed.

Applicant has amended the drawings with the attached replacement drawings containing the legend "Prior Art."

The present invention resides in the field of cable and wireless communications that require a realization of a stable clock recovery from a quadrature modulation signal. The present invention is directed to addressing problems that have previously occurred with conventional error selection circuits applied to binary digital signals in a digital signal player that plays information recorded on a recording medium such as DVD and requires symbol synchronization at the head of a frame, with frequency shift in received signal, during burst transmission using modulated signals in a frame format.

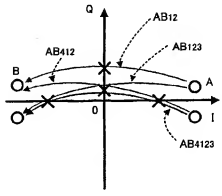
An example of the problems addressed can be seen in a signal transition with an additive +45° phase shift and noise in a detected signal wherein the signal points will disburse with additive noise and widen the level of the signal transition as follows:

FIG. 10



A detected signal, from the above Figure 10, in crossing the I/Q axis is schematically shown as follows:

FIG. 11



Note, the subscripts in the transition AB refer to the first through fourth quadrants. As can be seen in Figure 12, at least two zero crossing signals occur per symbol period owing to the arc shaped signal transition. As can be appreciated, in the case of two zero crossing signals occurring at regular intervals per symbol period, false or pseudo I patterns can be captured so that a clock recovery with a conventional error selection circuit will be unstable.

The present invention employs a clock recovery circuit capable of both a fast and accurate clock phase locking, even in the presence of frequency shift and noise.

Two embodiments of our invention are schematically shown in Figures 1 and 27.

In operation, an input signal can include a preamble with an alternating bit sequence pattern, a unique word, and the desired data. A detection unit detects zero crossings and measures the time interval therebetween. A judgment unit can determine when an interval signal is within a predetermined range and a second judgment unit can sum two adjacent interval

signals and judge whether the two interval signals are within a predetermined range. A control unit controls the zero crossing signal based on the judgment results and outputs a valid zero-crossing signal if judged in the affirmative. A switching unit switches between outputting the zero-crossing signal and the valid zero-crossing signal as valid phase error information based on a frame reception signal input from a frame detection unit. A clock generation unit uses the valid phase error information in generating the desired symbol clock.

In summary, our present invention detects a "N zero-crossing interval" and a judgment is made as to whether the duration of the N zero-crossing interval is within a predetermined acceptable interval range. This structure enables, even when frequency slippage occurs in the received signal, to still achieve a desired effect of selecting accurate phase error information, that is likely to be accurate, and as a result, enable recovering a stable clock and decrypting data with the use of the clock, without invalidating both the zero-crossing signal on the in-phase axis and a zero-crossing signal on the quadrature axis.

Our amended claims both resolve problems in the prior art's effort of realizing a stable recovery from a quadrature modulation signal and emphasize a difference over an FM demodulation method of improving a signal to noise ratio.

The Office Action rejected Claims 1, 2, 5-9, 15 and 16 as being obvious over applicant's admitted prior art in Figure 37 and Figure 4, when taken in combination with the teaching of *Takeda et al.* (U.S. Patent No. 4, 551,846).

Basically, *Takeda et al.* is directed to a detection of low signal to noise ratio communications with low distortion by utilizing an integrated circuit. This is set forth in Column 2, Line 66 to Column 3, Line 5, as follows:

> A FSK communication system is generally used in data communication. Such a system belongs to a so-called frequency modulator-demodulator system in which signals having different sine wave frequencies are sent or received in correspondence to a digitized binary signal of one or zero. Such a frequency system is primarily used as an acoustic coupled modem or a low speed modem.

Takeda et al. teaches a use of a plurality of N counters, each of which are activated, that is started and stopped at a zero-cross interval, and which is shifted by one period from the start and stop of the next counter in the sequence. Purpose of this circuit is to increase a signal to noise ratio by a factor of by the number of counters. Such an approach, however, has an inherent distortion which is addressed in the *Takeda et al.* reference by providing a demodulated output which changes not at a zero cross point in the FSK signal, but at a point delayed by a suitable amount.

A teaching, appreciated by a person of ordinary skill in this field, from the *Takeda et al.* reference would be represented by the schematic circuit shown in Figure 7, with a demodulated output having reduced distortion by outputting the demodulated signal with a suitable delay time, based on a comparison signal.

Claims 3, 10, 12 and 13 were further held to be obvious, again over applicant's admitted prior art, in view of the *Takeda et al.* reference, when further taken in view of *Kim* (U.S. Patent No. 5,859,671).

Kim was basically cited to teach a clock recovery circuit shown in Figure 1, and described in Column 1, Lines 38-51.

As can be appreciated, *Kim* was directed to a symbol timing recovery circuit for digital television when an analog signal from a tuner is converted to digital data by a symbol clock having twice a symbol rate, fs. A digital demodulator recovers the digital data from an A/D

converter to a baseband signal as the transmission data. The digital demodulator can use a digital frequency and a phase locked loop. A matching filter circuit adjusts the symbol rate to be matched with a segment synchronizing signal detector. The segmented signal generated from the matching circuit is applied to a signal processor at the next stage and simultaneously supplied to the segment synchronization signal detector. A phase error detector can detect a phase difference between first to fourth synchronizing symbols and a symbol clock phase adjuster can then adjust the phase of a symbol clock by the phase error signal generated and supplies the adjusted symbol clock to the A/D converter.

It is respectfully submitted that in view of the newly submitted claim amendments, applicant has more than adequately distinguished over any hypothetical combination relied upon in the Office Action rejection. Other than relying upon the teachings of our present invention and disregarding the difference in the technology used by our present invention in recovering a clock signal from a quadrature modulation signal, such a hypothetical combination of reference would fail to render our present claims obvious.

> It is the Examiner's burden to establish *prima facie* obviousness. *See In re Rijckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993) Obviousness requires a suggestion of all the elements in a claim *(CFMT, Inc. v. Yieldup Int'l Corp.,* 349 F.3d 1333, 1342 (Fed. Cir. 2003)) and "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Here, we find that the Examiner has not identified all the elements of claim 1, nor provided a reason that would have prompted the skilled worker to have arranged them in the manner necessary to reach the claimed invention.
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> *Ex parte* Karoleen B. Alexander, No. 2007-2698, slip op. at 6 (B.P.A.I. Nov. 30, 2007)

The Office Action further rejected Claims 4 and 11 as being obvious over our admitted prior art in view of the *Takeda et al.* reference when further taken in view of *Bolger et al.* (U.S. Patent No. 5,565,930).

Bolger et al. teaches an output of a circuit 30 in Figure 4 (see Column 9, Lines 38-45) for generating a pulse at the center of an adjacent zero-crossing with a reference to a valid crossing signal for the purpose of adjusting the timing of a generated symbol clock. The Office Action then concluded that it would be obvious to use a phase error associated with a generated pulse to adjust timing in a symbol clock.

Bolger et al. was basically cited for teaching signal processing in a quadrature phasing in an attempt to make up for the deficiencies of the *Takeda et al.* disclosure. More specifically, *Bolger et al.* was attempting to recover suppressed digital signals buried in an analog television signal. Purportedly, the *Bolger et al.* inventors discovered the ability of a Sigma-Delta architecture for solving problems of analog to digital conversion encountered after detecting a relatively low-power binary phase-shift-keyed (BPSK) modulation of a suppressed carrier having the same frequency as the video character in the quadrature phasing therewith.

The solution suggested was digitization of the detected BPSK with an oversampling analog-to-digital converter to increase the number of bits resolution with a relatively inexpensive flash converter. It was recognized that the BPSK had a relatively low amplitude compared to the maximally interfering analog television signal remnants, and in this manner could be constructed so it would not be overwhelmed by the quantizing noise.

Applicant submits that any combination of references that must be modified beyond their functions is suggestive of an unintended use of hindsight that may have been utilized to drive the

present rejection. This is particularly true for an Examiner who is attempting to provide a diligent effort that only patentable subject matter occurs. The *KSR* Guidelines do not justify such an approach. There is still a requirement for the Examiner to step back from the zeal of the examination process and to appreciate that a Patent Examiner has to wear both hats of advocating a position relative to the prior art while at the same time objectively rendering in a judge-like manner a decision on the patentability of the present claims.

As set forth in MPEP 2142,

> To reach a proper determination under 35 U.S.C. §103, the examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

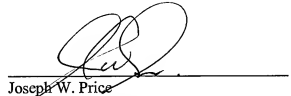
In summary, it is believed that the amended claims more than adequately place the present invention into an appropriate context, wherein a person of ordinary skill in the field would not seek or attempt to combine the diverse references relied upon in the previous rejection under 35 U.S.C. §103.

It is respectfully submitted that the case is now in condition for allowance and an early notification of the same is requested.

If the Examiner believes a telephone interview would assist in the prosecution of this case, the undersigned attorney can be contacted at the listed phone number.

Very truly yours,

SNELL & WILMER L.L.P.



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